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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/816,319 | 03/22/2001 | Wenbin Jiang | 3918P002X2 | 2293 |

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| EXAMINER | |
|---|---|
| SINGH, DALZID E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2633 | |

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/816,319 | JIANG ET AL. | |
| | Examiner | Art Unit | |
| | Dalzid Singh | 2633 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9,10,25,26 and 84-108* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,25,26 and 84-108* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10 September 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of restriction requirement in the reply filed on 15 November 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 9, 10, 25, 26 and 84-108 are rejected under 35 U.S.C. 102(e) as being anticipated by Scharf et al (US Patent No. 6,369,924).

Regarding claim 84, Scharf et al disclose optical transceiver module, as shown in Figs. 1-6, comprising:

an optical block (25 shown in Fig. 6) having a first opening to receive a first optoelectronic device (the optoelectronic device (44 or 45) is shown in Fig. 6);

the first optoelectronic device (44 or 45) coupled into the first opening (see col. 5, lines 26-33);

a motherboard printed circuit board (22 shown in Fig. 1; see col. 4, lines 16-18);

a first daughterboard printed circuit board (PCB) coupled to terminals of the first optoelectronic device in parallel to a first optical axis of the first optoelectronic device (26, 27 shown in Figs. 3 and 6 shows daughterboards coupled to the optoelectronic device (44 and 45)), the first daughterboard printed circuit board coupled at a first angle to the motherboard printed circuit board (as shown in Fig. 1, the daughterboard is coupled to the motherboard; see col. 5, lines 60-64; as shown in Fig. 6, the daughterboard is positioned in an angle).

Regarding claim 85, in col. 4, lines 18-21, Scharf et al disclose housing coupled to the motherboard printed circuit board.

Regarding claim 86, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the housing is a shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference (EMI).

Regarding claim 87, as shown in Fig. 6, Scharf et al show that the first angle is substantially ninety degrees so that the first daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claims 88, 98 and 99, the motherboard printed circuit board has a plurality of pins to couple to an external printed circuit board (since the motherboard or mounting board may be coupled to other devices, therefore the mother board has pins to coupled to such devices; see col. 4, lines 25-27).

Regarding claim 89, in Fig. 2, Scharf et al show the motherboard printed circuit board has a connector to couple to a connector of an external printed circuit board.

Regarding claim 90, in Figs. 1-6, Scharf et al show the first daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board.

Regarding claim 91, in col. 5, lines 57-64, Scharf et al disclose that the traces of first daughterboard printed circuit board are coupled traces of the motherboard printed circuit board by solder joints.

Regarding claim 101, in col. 5, lines 57-64, Scharf et al disclose that the traces of first daughterboard printed circuit board are coupled traces of the motherboard printed circuit board by solder joints, and the traces of second daughterboard printed circuit board are coupled traces of the motherboard printed-circuit board by solder joints.

Regarding claim 92, as shown in Fig. 6, Scharf et al show that the optical block further having a second opening to receive a second optoelectronic device (44 or 45), and wherein the fiber optic module further comprises, a second optoelectronic device coupled into the second opening, and a second daughterboard printed circuit board (PCB) (26 or 27) coupled to terminals of the second optoelectronic device in parallel to a second optical axis of the second optoelectronic device, the second daughterboard printed circuit board coupled at a second angle to the motherboard printed circuit board.

Regarding claim 93, in col. 5, lines 26-33, Scharf et al disclose that the fiber optic module is a fiber optic transceiver and the first optoelectronic device is a transmitter (emitter) to couple photons into a first optical fiber, and the second optoelectronic device is a receiver to receive photons from a second optical fiber.

Regarding claim 94, in col. 4, lines 18-21, Scharf et al disclose a housing coupled to the motherboard printed circuit board.

Regarding claim 95, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the housing is a shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference.

Regarding claim 96, as shown in Fig. 6, Scharf et al show that the first angle is substantially ninety degrees so that the first daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claim 97, as shown in Fig. 6, Scharf et al show that the second angle is substantially ninety degrees so that the second daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claim 100, in Figs. 1-6, Scharf et al show the first daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board, and the second daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board.

Regarding claim 102, in col. 4, lines 18-21, Scharf et al disclose housing having an opening at an end coupled to the motherboard printed circuit board.

Regarding claim 103, the first daughterboard printed circuit board and the second daughterboard printed circuit board each have a connector to couple to a connector of a host system printed circuit board through the opening at the end of the housing (since the motherboard or mounting board may be coupled to other devices, therefore the mother board has pins to coupled to such devices; see col. 4, lines 25-27).

Regarding claim 104, shown in Fig. 1, the motherboard printed circuit board includes an inner septum to separate the fiber optic module into a first side and a second side (shown in Fig. 1 is the separation of pins on either side).

Regarding claim 105, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the inner septum is a conductive shield to reduce crosstalk electromagnetic radiation.

Regarding claim 106, in Fig. 6, Scharf et al show a housing having an inner septum to separate the fiber optic module into a first side and a second side, the housing coupled to the motherboard printed circuit board .

Regarding claim 107, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the housing is a conductive shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference (EMT) and the septum is a conductive shield to reduce crosstalk electromagnetic radiation.

Regarding claim 108, as shown in Fig. 6, Scharf et al show the first and second daughterboard printed circuit boards are vertical printed circuit boards and the motherboard printed circuit board is a horizontal motherboard printed circuit board.

Regarding claim 9, in col. 5, lines 10-15, Scharf et al disclose that the first daughterboard printed circuit board further comprises a ground plane to reduce electro-magnetic fields generated by the electrical components.

Regarding claim 10, in col. 5, lines 10-15, Scharf et al disclose that the second daughterboard printed circuit board further comprises a ground plane to reduce electro-magnetic fields generated by the electrical components.

Regarding claim 25, in col. 5, lines 1-25, Scharf et al disclose that the first daughterboard printed circuit board further comprises:

first electrical components coupled between the first optoelectronic device and the motherboard printed circuit board on a first side of the first daughterboard in printed circuit board, the first electrical components for controlling the first optoelectronic device, and a first ground plane coupled to a second side of the first daughterboard internal printed circuit board to reduce electro-magnetic fields; and,

wherein the second daughterboard in printed circuit board further comprises: second electrical components coupled between the second optoelectronic device and the motherboard printed circuit board on a first side of the second internal printed circuit board, the second electrical components for controlling the second optoelectronic device.

Regarding claim 26, in col. 5, lines 1-25, Scharf et al disclose that the second daughterboard sprinted circuit board further comprises: a second ground plane coupled to a second side of the second internal printed circuit board to reduce electro-magnetic fields.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McGinley et al (US Patent No. 5,528,408) is cited to show optoelectronic transceiver.

Wolf (US Patent No. 6,024,500) is cited to show transceiver package.

Gilliland et al (US Patent No. 6,160,647) is cited to show optoelectronic transmitter.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalzid Singh whose telephone number is (571) 272-3029. The examiner can normally be reached on Mon-Fri 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272--3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

06 August 2005
Dalzid Singh